REMARKS

After entry of this Amendment, claims 4-13, 18, 19, 21-24, 31-42, 44-46, and 51-71 will be pending in this application; claims 32, 37, 39, 44, and 46 have been amended. Support for the amendments may be found throughout the Specification, at least in Figures 3 and related text, and in the originally filed claims.

Objections to Claims

Claims 32, 37, 39, 44, and 46 are objected to for informalities. Applicants respectfully submit that the foregoing amendments fully address the objections to these claims.

Rejection of Claims under 35 U.S.C. § 251

Claims 4-13, 18, 19, 21-24, 31-42, 44-46, and 51-71 are rejected under 35 U.S.C. § 251 as being based upon a defective reissue oath/declaration. Applicants respectfully submit that the substitute reissue oath/declaration accompanying this paper is fully responsive to this rejection.

Rejection of Claims under 35 U.S.C. § 102

Claim 31 is rejected under 35 U.S.C. § 102(b) as being unpatentable over U.S. Patent No. 3,701,119 to Waaben et al. ("Waaben"). Waaben appears to disclose a transistor and diode-based switch for use with semiconductor memories. *See* Waaben, Fig. 1 and related text. The examiner relies on Waaben to teach all of the limitations of independent claim 31.

Waaben does not, however, teach or suggest address circuitry for disabling all but a selected one of the first set of conductive lines, wherein the address circuitry comprises a first pattern of rectifiers directly connected to a first set of conductive lines, as required by independent claim 1. Rather, Waaben discloses a plurality of control circuits 12, which include, *inter alia*, charge storage diode 16, first Schottky-barrier diode 18, and second Schottky-barrier diode 20. Each control circuit 12 is connected to a digit line 14, and acts as an "automatic, self-opening switch" during "readout and detection of information stored in a selected memory cell 36" connected to digit line 14. *See* Waaben, column 2, lines 43-61 and column 3, line 53 – column 4, line 15. Control circuits 12 do not perform any addressing function in Waaben; instead, they simply decrease the potential of an already-selected digit line 14 to facilitate the

detection of the bit information stored in the already-selected memory cell 36 connected to the digit line 14. In other words, control circuits 12 are activated only after a particular digit line 14 has been selected, and do not perform any of the addressing required to actually make the selection. *See* Waaben, column 3, lines 6-18 and 53-65. Indeed, even if Waaben did disclose some way of addressing a particular memory cell 36, control circuits 12 (and the diodes therein) could not participate in such addressing, since they are activated only after a particular memory cell 36 has been selected. Therefore, Waaben's control circuits 12 do not and cannot disable all but a selected one of a first set of conductive lines, as required by independent claim 31.

Claim 31 is rejected under 35 U.S.C. § 102(b) as being unpatentable over U.S. Patent No. 4,608,672 to Roberts et al. ("Roberts"). Roberts appears to disclose a semiconductor memory with an address decoder in the center of the data field. *See* Roberts, column 1, lines 10-16. The Examiner relies on Roberts to teach all of the limitations of independent claim 31.

Roberts does not, however, teach or suggest address circuitry comprising a first pattern of rectifiers directly connected to a first set of conductive lines (which, along with a second set of conductive lines, define storage locations at intersections therebetween), as required by independent claim 1. Rather, Roberts discloses only NAND gates (e.g., NAND gate 50) connected to word lines (e.g., WL 58) which, in turn, connect to diodes (e.g., diodes 82, 84) in a memory array. *See* Roberts, Figs. 2 and 3 and related text. Notably, the diodes in address decoder 12 — e.g., Schottky diode 198 of Fig. 3 indicated by the Examiner — connect only to the NAND gates and internal $\overline{WL}$ lines (e.g., line 54) and do not connect to left memory array 20 or right memory array 22. *Ibid.* Rather, the diodes in address decoder 12 provide inputs to "word line driver 14 and the NAND gates thereof," which then vary the voltage on word line 58 (which connects to diodes 82, 84). *See* Roberts, column 4, line 38 – column 5, line 6. Thus, Roberts does not and cannot teach or suggest address circuitry comprising a first pattern of rectifiers connected to a first set of conductive lines, as required by independent claim 31.

Applicants submit that independent claim 31 and claims dependent therefrom are allowable for at least this reason.

CONCLUSION

In light of the foregoing, Applicants respectfully submit that all claims are now in condition for allowance.

Applicants believe that no additional fees are necessitated by the present Response. However, in the event that any additional fees are due, the Commissioner is hereby authorized to charge any such fees to Deposit Account No. 07-1700.

If the Examiner believes that a telephone conversation with Applicants' agent would expedite allowance of this application, the Examiner is cordially invited to call the undersigned.

Respectfully submitted,

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